

**Amendments to the Claims:**

This listing of claims will replace all prior versions and listings of claims in the application:

**Listing of the Claims:**

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1. (Currently Amended) A method including:

detecting a power management event in a system that includes a change in a system power between an external power source and a battery source; and

dynamically adjusting, in response to the power management event, a voltage level and clock frequency level provided to a plurality of system components including a microprocessor and system buses, including adjusting a chipset buffer strength.
2. (Canceled).
3. (Previously Presented) The method of claim 1, wherein a system chipset drives the system buses.
4. (Cancelled)

5. (Previously Presented) The method of claim 1, wherein the components include a memory subsystem and a graphics subsystem.

6. (Previously Presented) The method of claim 1, wherein the dynamically adjusting includes adjusting performance states of the plurality of system components between a high level and a low level.

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7. (Canceled).

8. (Currently Amended) The method of claim 17, wherein adjusting the performance state of a graphics subsystem includes selecting one predetermined level from two predetermined AGP Specification graphics performance levels.

9. (Currently Amended) The method of claim 6, wherein dynamically adjusting the performance states includes automatically placing the system in the a deep sleep state upon the occurrence of the power management event to adjust the performance states of the system components.

10-18. (Canceled)

19. (Currently Amended) A system comprising:

a detector adapted to detect generation of a power management event that includes a change in a system power between an external power source and a battery source; and

a controller to automatically adjust, in response to the power management event, voltage level and clock frequency level provided to a plurality of system components including a microprocessor and system buses, and to adjust a chipset buffer strength.

20. (Canceled).

21. (Previously Presented) The system of claim 19, wherein a system chipset drives the system buses.

22. (Cancelled)

23. (Previously Presented) The system of claim 19, wherein the components include a memory subsystem and a graphics subsystem.

24. (Previously Presented) The system of claim 19, wherein the dynamically

adjusting includes adjusting performance states of the plurality of system components between a high level and a low level..

25. (Canceled).

26. (Previously Presented) The system of claim 24, wherein adjusting the performance state of a graphics subsystem includes selecting one predetermined level from two predetermined AGP Specification graphics performance levels.

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27. (Currently Amended) The system of claim 24, wherein the low activity state-level is the-a deep sleep state.

28. (Currently Amended) An apparatus comprising:  
a detector adapted to detect generation of a power management event that includes a change in a system power between an external power source and a battery source; and  
a controller to automatically adjust, in response to the power management event, voltage level and clock frequency level provided to a plurality of system components including a microprocessor and system buses, and to adjust a chipset buffer strength.

29. (Canceled).

30. (Previously Presented) The apparatus of claim 28, wherein a system chipset drives the system buses.

31. (Cancelled)

32. (Previously Presented) The apparatus of claim 28, wherein the components include a memory subsystem and a graphics subsystem.

33. (Previously Presented) The apparatus of claim 28, wherein the dynamically adjusting includes adjusting performance states of the plurality of system components between a high level and a low level.

34. (Canceled).

35. (Previously Presented) The apparatus of claim 33, wherein adjusting the performance state of a graphics subsystem includes selecting one predetermined level from two predetermined AGP Specification graphics performance levels.

36. (Currently Amended) The apparatus of claim 33, wherein the low ~~activity~~

state level is the a deep sleep state.

37. (Currently Amended) A computer-readable medium having stored thereon a set of instructions to translate instructions, the set instructions, which when executed by a processor, cause the processor to perform a method comprising:

detecting a power management event that includes a change in a system power between an external power source and a battery source; and dynamically adjusting, in response to the power management event, a voltage level and clock frequency level provided to a plurality of system components including a microprocessor and system buses, including adjusting a chipset buffer strength.

38. (Canceled).

39. (Previously Presented) The computer-readable medium of claim 37, wherein a chipset drives the system buses.

40. (Previously Presented) The computer-readable medium of claim 37, further includes adjusting a chipset buffer strength.

41. (Previously Presented) The computer-readable medium of claim 37, wherein the components Currently Amended a memory subsystem and a graphics subsystem.

42. (Previously Presented) The computer-readable medium of claim 41, wherein the dynamically adjusting includes adjusting performance states of the plurality of system components between a high level and a low level.

43. (Canceled)

44. (Previously Presented) The computer-readable medium of claim 42, wherein adjusting the performance state of a graphics subsystem includes selecting one predetermined level from two predetermined AGP Specification graphics performance levels.

45. (Currently Amended) The computer-readable medium of claim 42, wherein dynamically adjusting the performance states includes automatically placing the system in the-a deep sleep state upon the occurrence of the power management event to adjust the performance states of the system components.